This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Previously Presented) A self-contained microprocessor subsystem for use in a system-on–chip (SoC) integrated circuit (IC) comprising a processor device, a SoC IC communications bus device and standardized components for enabling communications, said self-contained microprocessor sub-system comprising:

a plurality of processor core assemblies, each processor core assembly comprising:

two or more microprocessor devices each capable of performing operations to implement a given processing functionality;

a storage device associated with said two or more microprocessor devices in said processor core assembly for storing at least one of data and instructions in said processor core assembly; and,

a first local interconnect means residing in each said processor core assembly for enabling communication of instructions and data between said two or more microprocessor devices; and,

a second local interconnect means for enabling communications between said plurality of processor core assemblies; and,

a bridging device implementing a common macro for enabling send and receive data communications between said second local interconnect means of said self-contained microprocessor sub-system and said SoC IC communications bus device, whereby said plurality of processor core assemblies may communicate with standardized components of said SoC IC via said bridging device, whereby self-contained microprocessor sub-system communications traffic is separated from communications traffic in said SoC without having to accommodate standardized components in said SOC system.

2. (Original) The microprocessor subsystem as claimed in Claim 1, wherein said two or more microprocessor devices of said single processor core assembly operate under program control to enable a specific set of functionalities.

3. (Previously Presented) The microprocessor subsystem as claimed in Claim 1, wherein said second local interconnect means comprises a switch fabric.

4. (Previously Presented) The microprocessor subsystem as claimed in Claim 1, wherein said second local interconnect means comprises a communications bus.

5. (Original) The microprocessor subsystem as claimed in Claim 2, wherein said SoC IC is a network processor assembly, said microprocessor subsystem implementing packet communications processing functionality.

6. (Previously Presented) The microprocessor subsystem as claimed in Claim 5, wherein said self-contained microprocessor sub-system further comprises one or more interface devices capable of receiving communications according to a network communications protocol including one or more from the group comprising: Fibre Channel, Gb Ethernet, Infiniband.

7. (Original) The microprocessor subsystem as claimed in Claim 6, wherein said network processor assembly is configured as one of a DSP, coprocessor, Hybrid ASIC, or other network processing arrangement, said network processing assembly comprising:

a network processing device, and

a high-speed local bus means for interconnecting components of said network processing assembly with said network processing device.

8. (Previously Presented) The microprocessor subsystem as claimed in Claim 7, wherein standardized components of said network processor assembly include one or more selected from the group comprising: an SRAM, a DDR controller, a PCI-X bridge, a direct memory access DMA device, a DMA controller, an on-chip peripheral bus (OPB) for interfacing with external components via one or more I/O interface devices, and a Medium Access Control (MAC) protocol device employed to provide a data link layer interface to an Ethernet local area network (LAN) system.

9. (Previously Presented) The microprocessor subsystem as claimed in Claim 1, wherein said bridging device comprises a programmable processor local bus bridge device for enabling

data flow between the self-contained microprocessor subsystem and said communications bus device of said SoC IC.

10. (Previously Presented) The microprocessor subsystem as claimed in Claim 9, wherein said programmable processor local bus bridge device adapts communications signals and signaling protocols between two communication systems communicating via said SoC IC device implementing said self-contained microprocessor subsystem.

11. (Previously Presented) The microprocessor subsystem as claimed in Claim 1, wherein said second local interconnect means comprises a crossbar switch for tying together independent thread groups corresponding to two or more microprocessor devices.

12. (Previously Presented) The microprocessor subsystem as claimed in Claim 1, wherein said local memory storage device associated with said two or more microprocessor devices in said self-contained microprocessor sub-system includes one or more of: a local SRAM memory, a memory cache, and an I-cache connecting the sub-processors together.

13. (Previously Presented) The microprocessor subsystem as claimed in Claim 8, wherein said two or more microprocessor devices of each said processor core assembly comprises means for polling a communications bus device of said SoC IC for handling processing of one or more network protocol communications.

14. (Previously Presented) A system-on–chip (SoC) Integrated Circuit (IC) network processor architecture comprising:

a network processor core for controlling SoC network processor functions among a plurality of SoC network processor components;

an SoC local system bus device for enabling communications among said SoC network processor components and said network processor core, one SoC network processor component comprising an independent, self-contained multiprocessor subsystem core comprising:

i) a plurality of processor core clusters implementing given functionalities;

ii) at least one memory storage device for storing at least one of data and instructions;

iii) local interconnect means for enabling high–speed communication between two or more microprocessor devices, and,

iv) a bridging device implementing a common macro for enabling send and receive data communications between said local interconnect means of said self-contained microprocessor sub-system and said SoC local system bus device,

wherein said independent, self-contained multiprocessor subsystem core provides multi-threading network processing capability.

15. (Previously Presented) The SoC IC network processor architecture as claimed in Claim 14, wherein said independent, self-contained SoC multiprocessor subsystem core further comprises one or more interface devices capable of receiving communications according to a network communications protocol including one or more from the group comprising: Fibre Channel, Gb Ethernet, Infiniband.

16. (Original) The SoC IC network processor architecture as claimed in Claim 15, configured as one of a DSP, coprocessor, Hybrid ASIC, or other network processing arrangement, wherein said SoC local system bus device is a high-speed local bus means for interconnecting said SoC network processor components with said network processing core.

17. (Original) The SoC IC network processor architecture as claimed in Claim 16, wherein said network processor components include one or more selected from the group comprising: an SRAM, a DDR controller, a PCI-X bridge, a direct memory access DMA device, a DMA controller, an on-chip peripheral bus (OPB) for interfacing with external components via one or more I/O interface devices, and a Medium Access Control (MAC) protocol device employed to provide a data link layer interface to an Ethernet local area network (LAN) system.

18. (Previously Presented) The SoC IC network processor architecture as claimed in Claim 14, wherein said bridging device comprises a programmable processor local bus bridge device

for enabling data flow between the microprocessor subsystem and said SoC local system bus device.

19. (Original) The SoC IC network processor architecture as claimed in Claim 18, wherein said programmable processor local bus bridge device adapts communications signals and signaling protocols between two communication systems communicating via said SoC IC device implementing said single multiprocessor subsystem core.

20. (Previously Presented) The SoC IC network processor architecture as claimed in Claim 14, wherein said local interconnect means of said single multiprocessor subsystem core comprises a crossbar switch for tying together independent thread groups corresponding to two or more microprocessor devices.

21. (Original) The SoC IC network processor architecture as claimed in Claim 14, wherein said at least one memory storage device associated with said two or more microprocessor devices in said sub-system includes one or more of: a local SRAM memory, a memory cache, and an I-cache for connecting the microprocessor devices together.

22. (Previously Presented) The SoC IC network processor architecture as claimed in Claim 21, wherein said independent, self-contained multiprocessor subsystem core comprises means for polling a local system bus device of said SoC IC for handling processing of one or more network protocol communications.

23. – 30. (Canceled)